REMARKS

Claims 1-5 and 7-25 are currently active.

The Examiner has rejected Claims 1-5, 7-17 and 19 under 35 U.S.C. 112, second paragraph. The claims have been amended to obviate this rejection. Please note in Claim 15, it already states the "width of the carrier mechanism."

The Examiner has rejected Claims 1-5, 15, 16 and 18-21 as being unpatentable over Haddock in view of Nelson. Applicant respectfully traverses this rejection.

In pertinent part, Haddock teaches m- bit wide receiver data paths 111a through 114a couple Macs 110a through 110n to path controller 120, wherein m = 16 bits. Path controller 120 is sliced into a number of sub path controllers. Likewise, path 111a through 114a are sliced into an equal number of n- bit wide receive data sub paths wherein n times the number of sub path controllers = m. See column 6, lines 16-29.

Each sub path belonging to a particular path as routed to a different sub path controller. The sub path controllers 120a through 120n are each coupled to packet memory 130 via their respective x-bit wide receiver data bus 121a to 121n, collectively data bus 121.

The width of data bus 121 connecting the sub path controllers to packet memory 130 is double the sum of the width of the receive and transmit data path coupling the Macs to path control 120. Thus, in the four sub path (4 slice) embodiment, the data bus 121 is 256 bits wide, while, the data bus 121 in the 8 sub paths (8 slice) embodiment is 512 bits wide. It is appreciated that in a 16 sub path configuration, the 1024 bit wide data bus connects sub path controllers to packet memory 130. See column 6, lines 30-53. The sub path controllers each contains separate receive buffers coupled to the sub path to receive data therefrom. In the receive data direction, each sub path controller accumulates at least x bits of data in the receive buffer from associated data sub path until they can transfer the bits of data to packet memory 130, wherein x is a multiple of n. likewise, sub path controller 120b receives slices of data packets from Macs 110a, 110b, 110c and 110n into receive buffers 228 through 220 d via sub paths 111a2, 112a2, 113a2, and 114a2. Receive buffers operate in serial-to-parallel bit stream converters, and burst x bits of data in parallel to packet memory. The x bits contain n-bit slices of a data packet received from the Mac connected to the corresponding sub path. See column 6, line 54-column 7, line 8.

As is clear from the above description, Haddock only teaches that a given sub path is defined in bits and each receive separate slices of data packets. See column 6, line 38. There is no teaching or suggestion anywhere of "said carrier mechanism having a width wider than the width of the input and output port mechanisms so data from more than one packet at a

time is transferred in the allocated time slots," as found in Claim 1. Every path or sub path has a width but there is nothing to indicate the any path needs this limitation of Claim 1. Furthermore, Claim 1 has the limitation that "said providing mechanism transferring more than one packet at a time in the allocated time slots whose total width equals the width of the carrier mechanism in each allocated time slot to the memory mechanism." In this way, there is most efficient use of the resources.

Furthermore, there is no teaching or suggestion of "said providing mechanism transferring more than one packet at a time to the memory mechanism in the allocated time slot only when there is enough data from more than one packet from an input stage queue group to fill the width but not transferring any data from any packets from the input stage queue groups in the allocated time slot when there is not enough data to fill the width of the carrier mechanism," as found in Claim 1. The statement that the Examiner relies upon in Haddock simply states that each sub path controller accumulates at least x bits of data in the receive buffer from its associated receive data sub path until it can transfer the bits of data to packet memory 130, wherein x is a multiple of the number of bits in the receive data sub path. See column 6, lines 57-61. Just by the simple use of the language of "at least" x bits, indicates that more than x bits can be accumulated and sent to packet memory 130, which means that there are times when only x bits, that is, less than the total number of bits that can be transferred, are transferred, and thus the width of the path is not filled, at such times.

Accordingly, for all of these reasons, Haddock does not meet any of the limitations that the examiner states they do. Since the primary reference the Examiner cites does not support the Examiner's position regarding the above quoted limitations, then the reference of Nelson which also does not teach or suggest these limitations, but that is cited by the Examiner for the proposition that it teaches to carry packets in the allocated time slot, in combination with Haddock fails to meet the limitations of applicant's claims. Accordingly, Claims 1-5, 15, 16 and 18-21 are patentable over Haddock in view of Nelson.

The Examiner has rejected Claims 7-14, 17 and 22-25 as being unpatentable over Haddock in view of Nelson and Fukano. Applicant had discussed Fukano in the previous Office Action. Fukano does not add anything to the teachings of Haddock or Nelson to arrive at the above quoted limitations. Accordingly, these claims are patentable over Haddock in view of Nelson and Fukano.

In view of the foregoing amendments and remarks, it is respectfully requested that the outstanding rejections and objections to this application be reconsidered and withdrawn, and Claims 1-5 and 7-25, now in this application be allowed.

Respectfully submitted,

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